

The diagram illustrates a security device 101 and its connection to a PC 140. The security device 101 includes a CPU 120a with general-purpose registers 119a and a general-purpose register controller 121. It also features an I/O port 122, a secret key storing register 107, and a security controller 111a. The security controller 111a contains a DMA 118a, a program decryption execute flag 112f, a RAM copy flag 113f, and a chip select dispatcher 114a. The device is connected to a PC 140 via a USB upstream port 125 and a bus port 110a. The PC 140 contains a program 128a and an encryption program 128b. The security device 101 also includes a public key storing register 106, a RAM 104, and a RAM 105.

FIG. 2

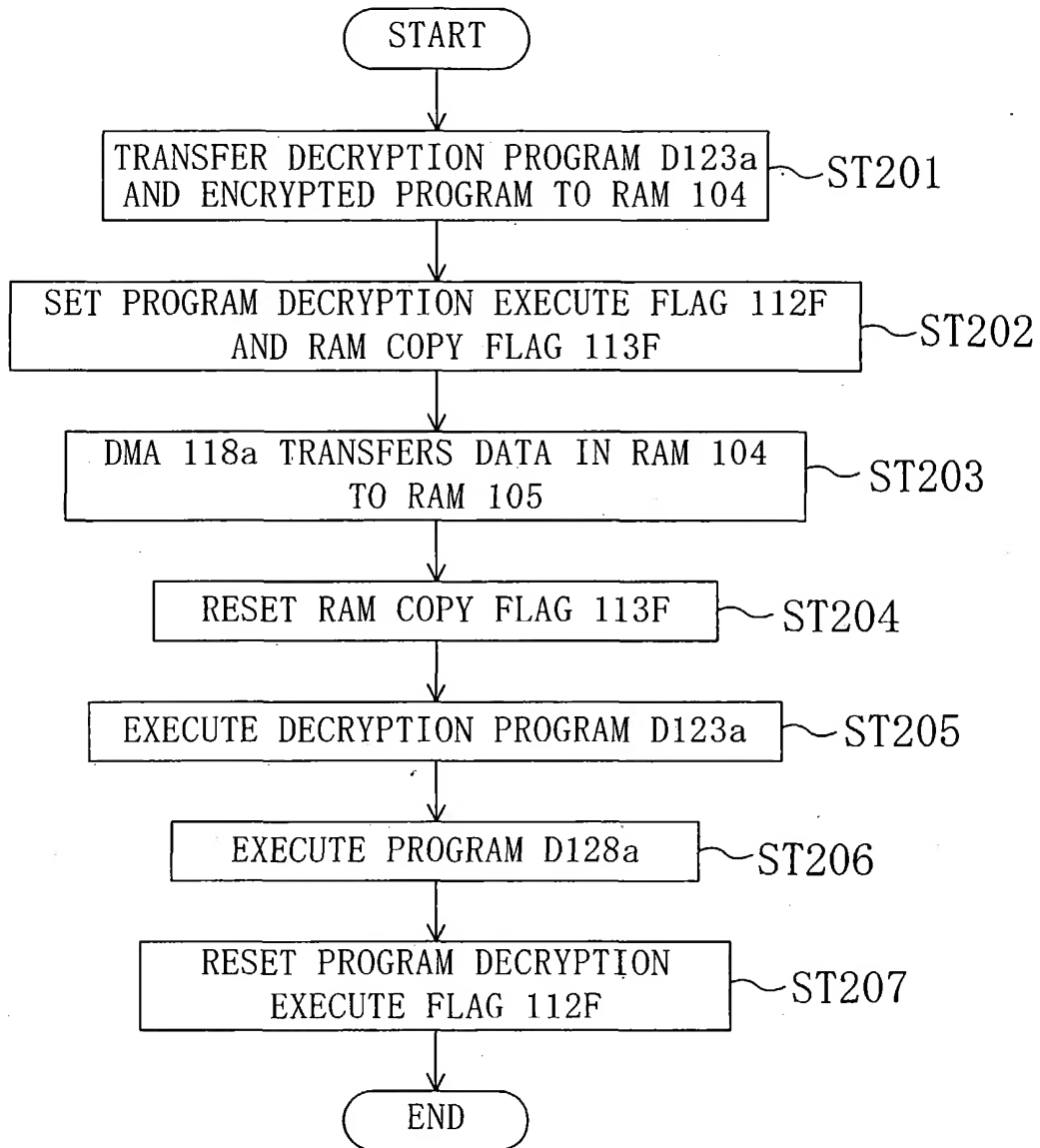


FIG. 3

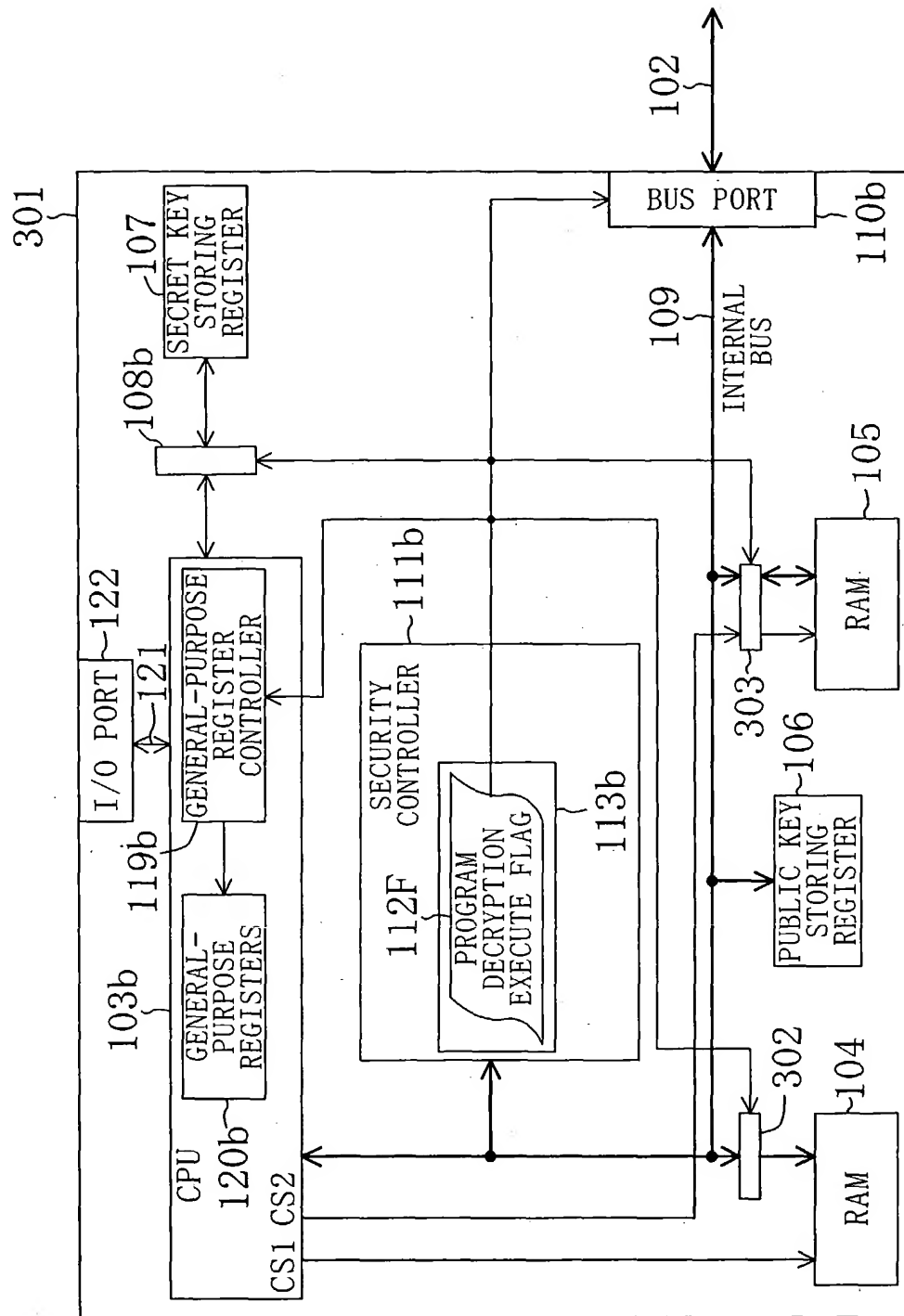


FIG. 4

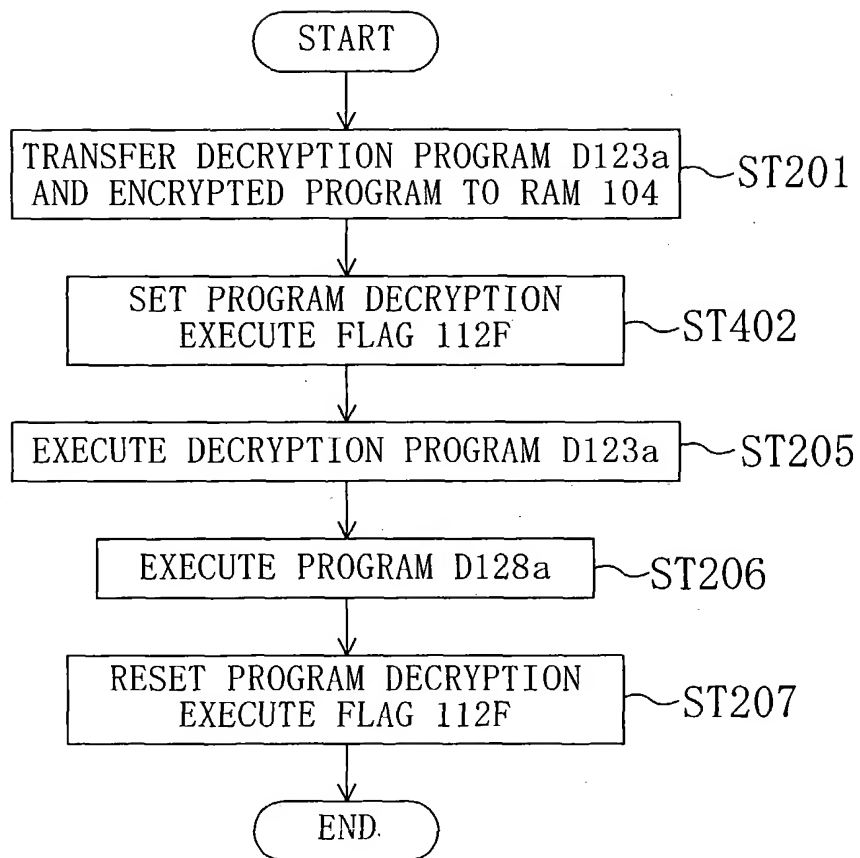


FIG. 5

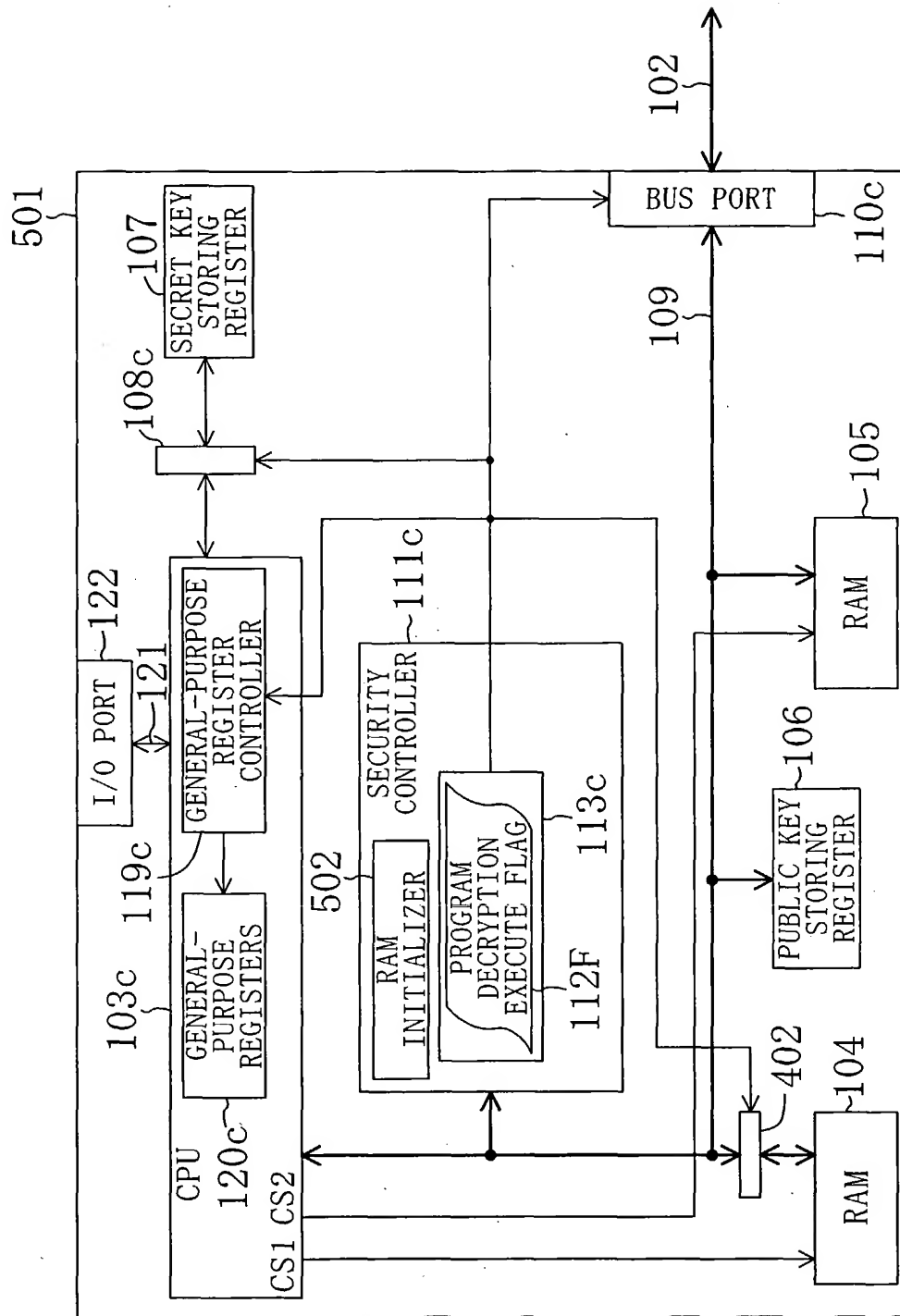


FIG. 6

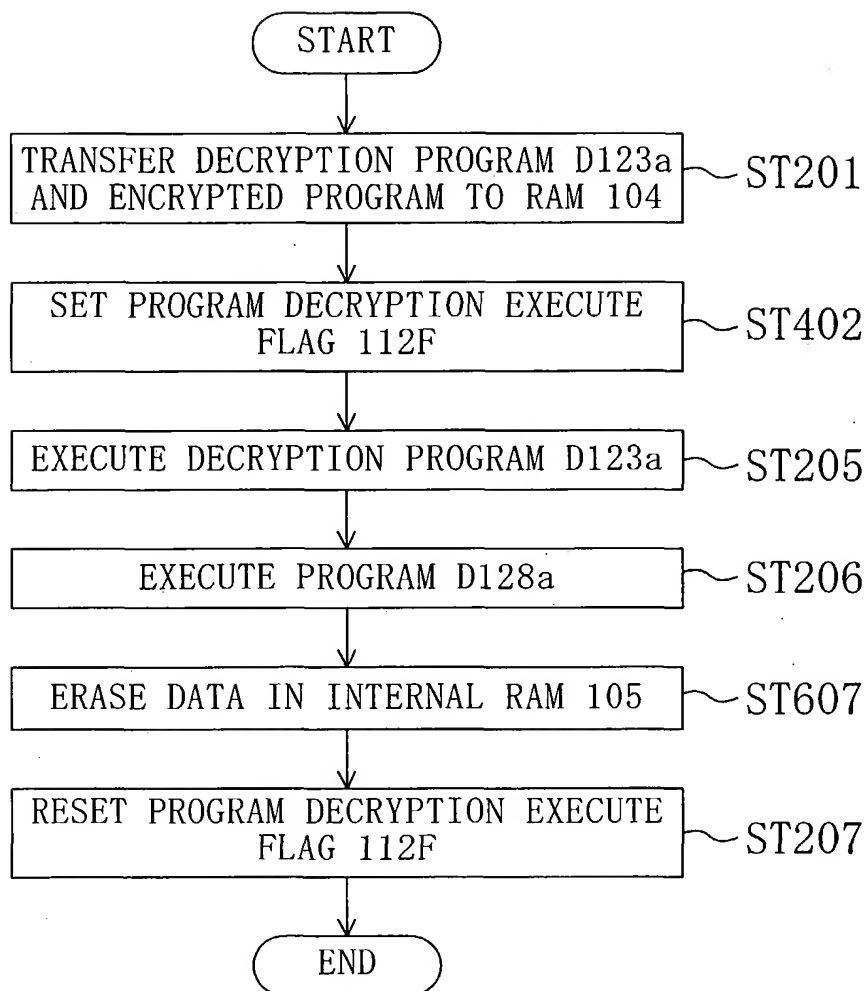


FIG. 7

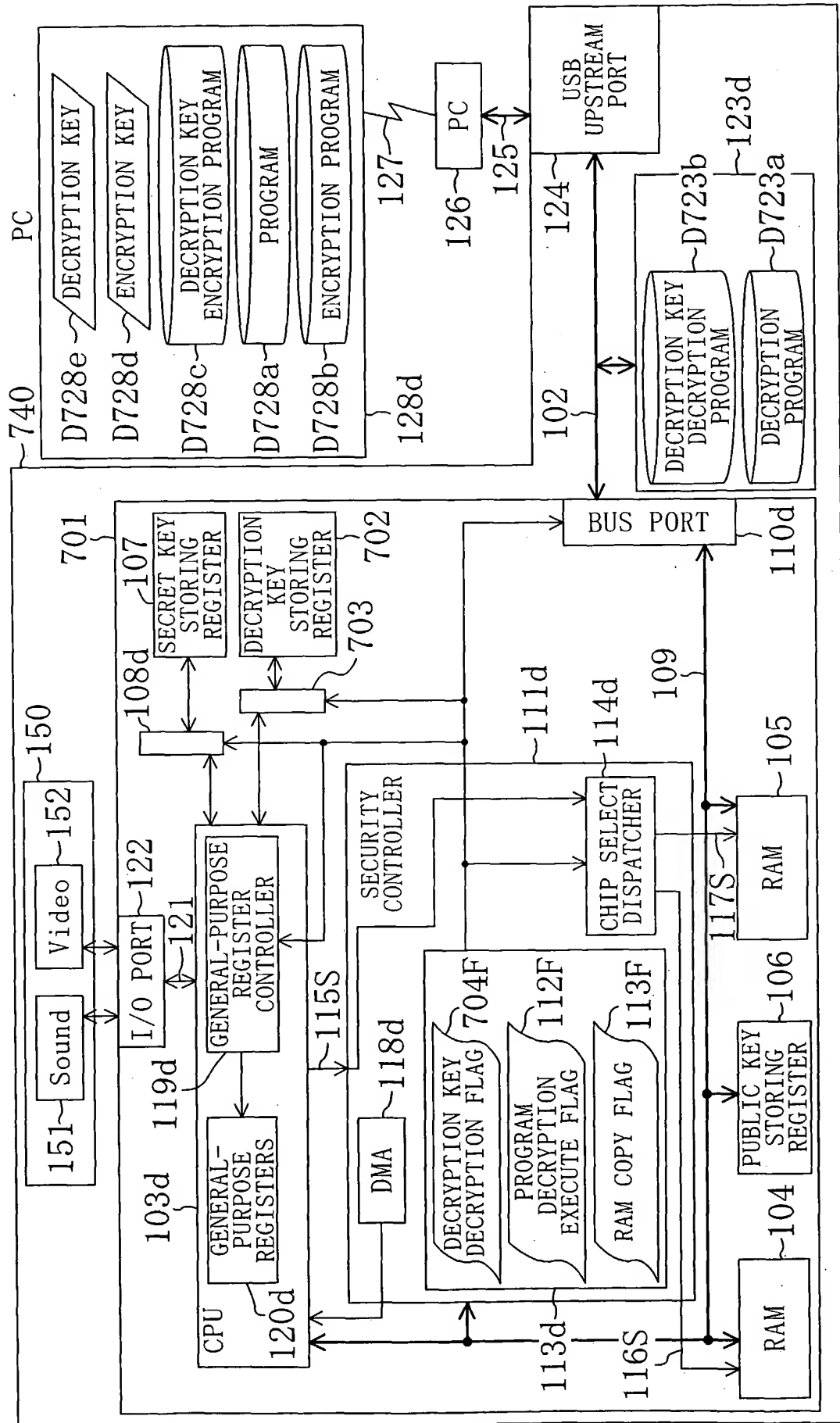


FIG. 8

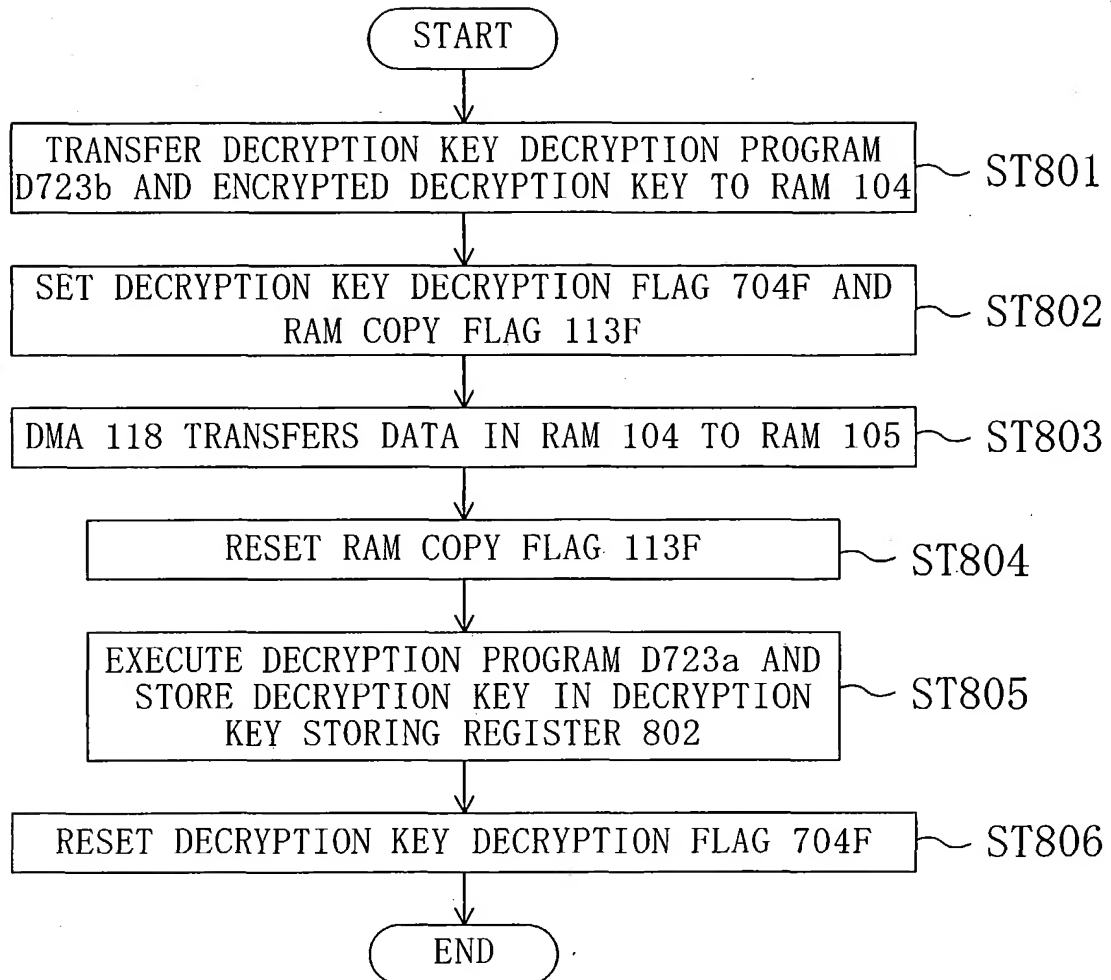




FIG. 9

RAM COPY FLAG 113F	0	1	0	1	0
DECRYPTION KEY DECRYPTION FLAG 704F	0	1	1	0	0
PROGRAM DECRYPTION EXECUTE FLAG 112F	0	0	0	1	1
BUS PORT 110d	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
SECRET KEY ACCESS PORT 108d	CLOSE	CLOSE	OPEN	CLOSE	CLOSE
DECRYPTION KEY ACCESS PORT 703	CLOSE	CLOSE	OPEN	CLOSE	OPEN
CHIP SELECT SIGNAL 116S	CS115	ASSERT	NEGATE	ASSERT	NEGATE
CHIP SELECT SIGNAL 117S	NEGATE	ASSERT	CS115	ASSERT	CS115

FIG. 10

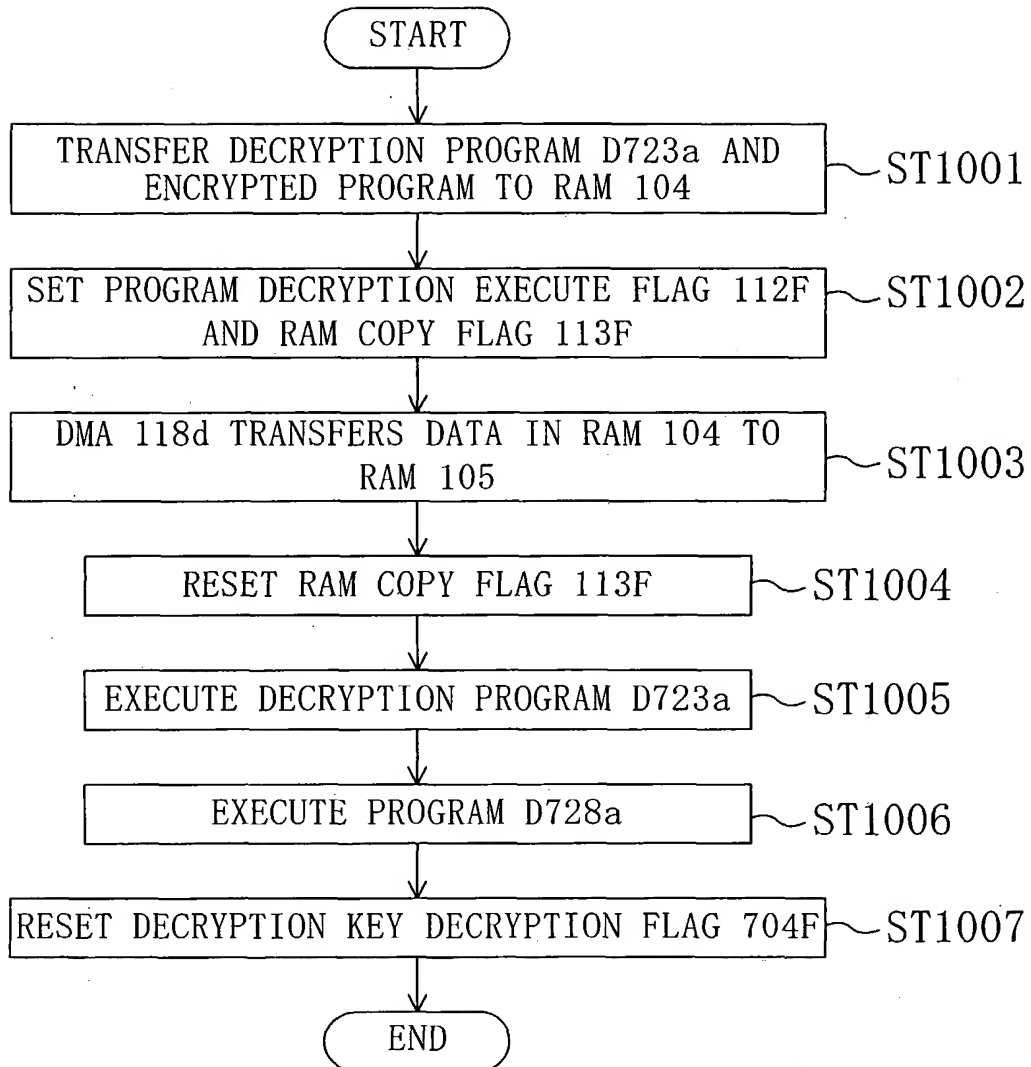


FIG. 11

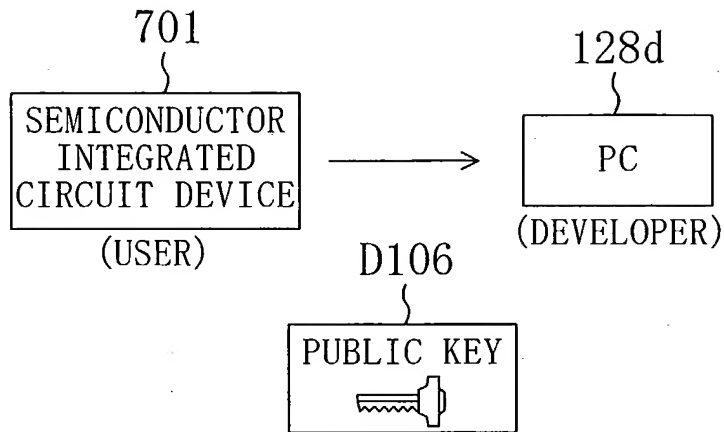


FIG. 12

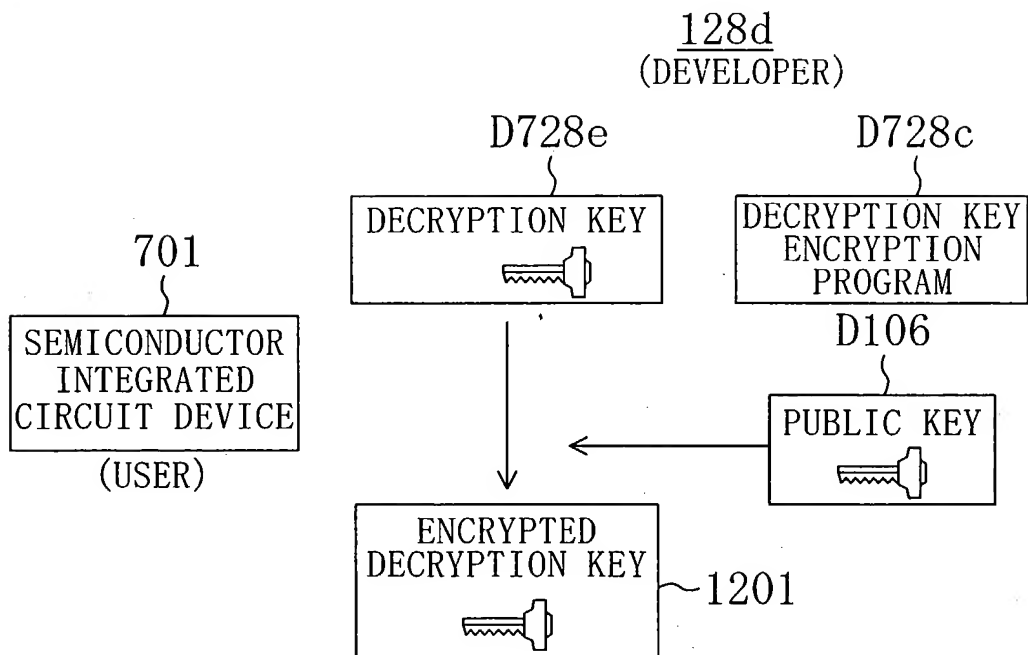


FIG. 13

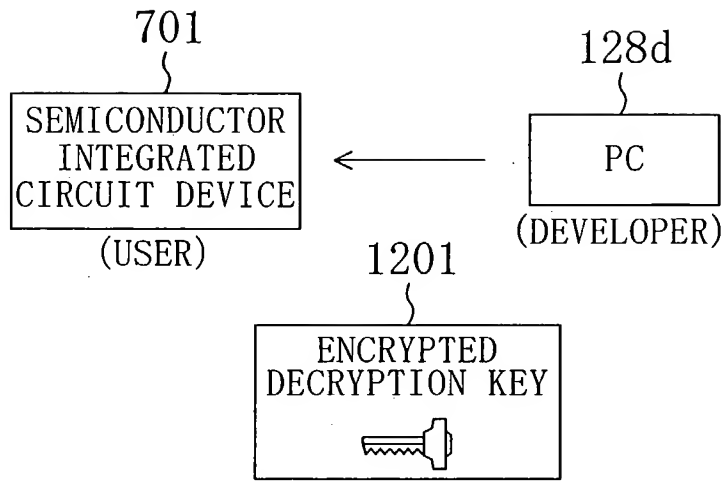


FIG. 14

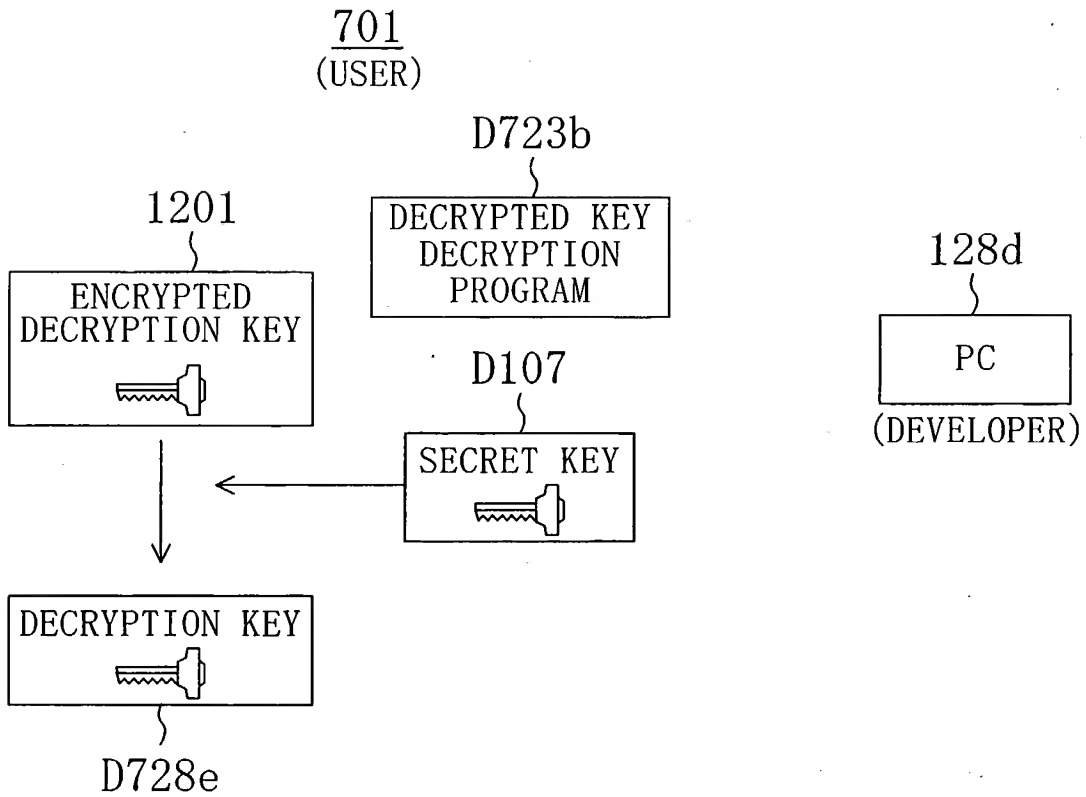


FIG. 15

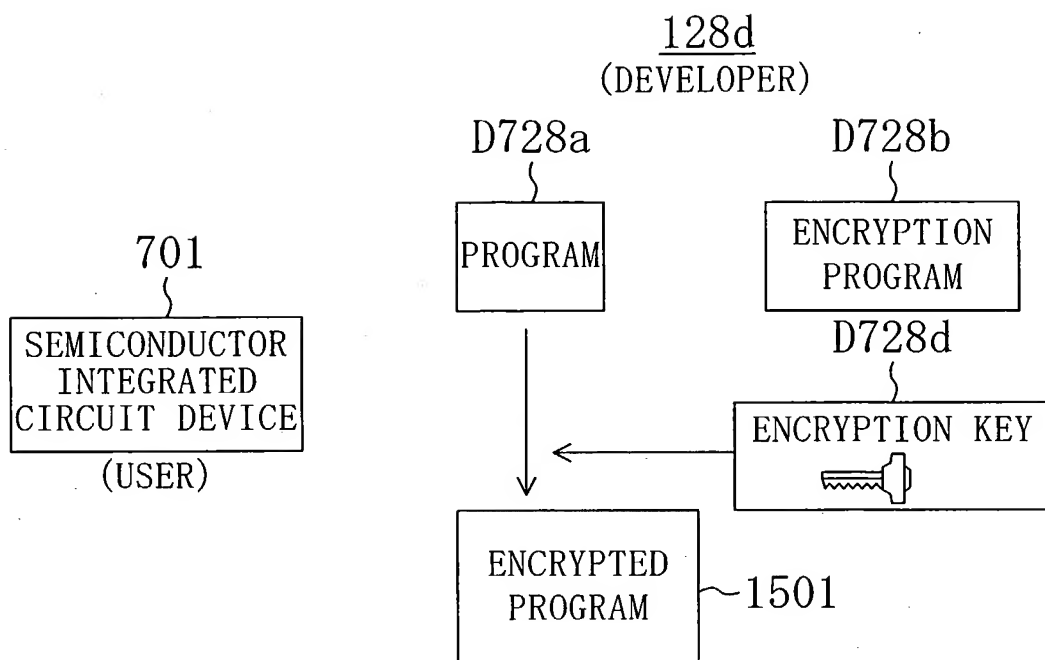


FIG. 16

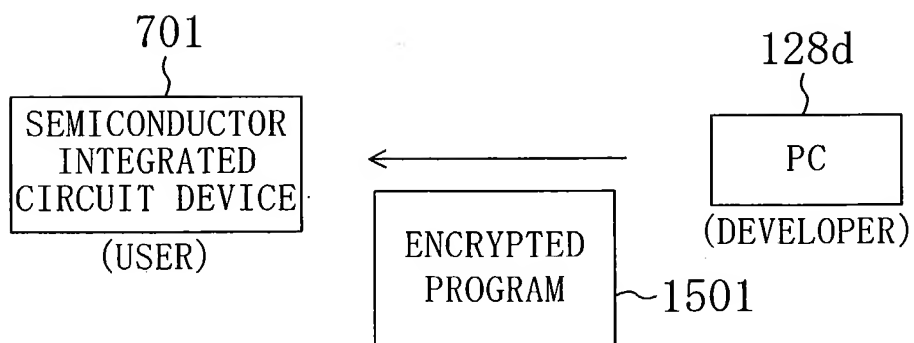


FIG. 17

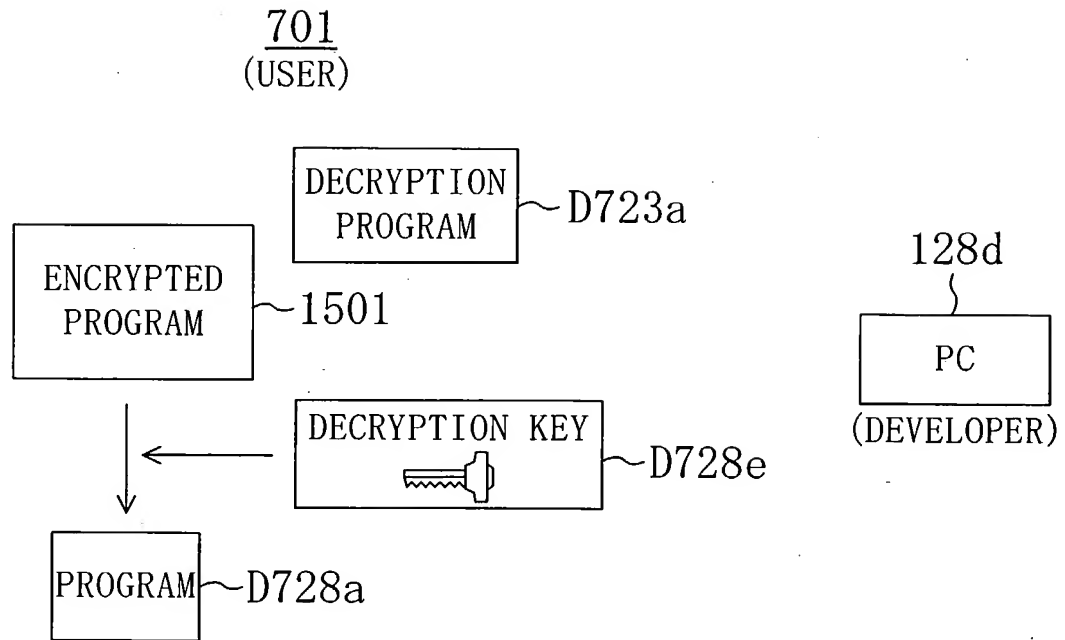


FIG. 18  
PRIOR ART

